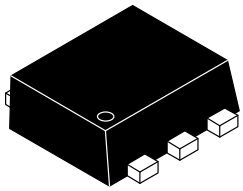
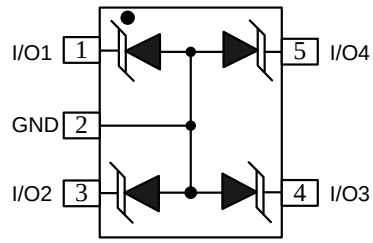
SOT-553



Features

- ► Solid-state silicon-avalanche technology
- ► 30 Watts Peak Pulse Power per Line (tp=8/20μs)
- ► Low operating and clamping voltages
- ► Up to Four (4) Lines of Protection
- ► Working Voltages: 5 V
- ► Low Leakage Current

PIN CONFIGURATION



Complies with the following standards

IEC61000-4-2

15 kV (air discharge)

8 kV(contact discharge)

Applications

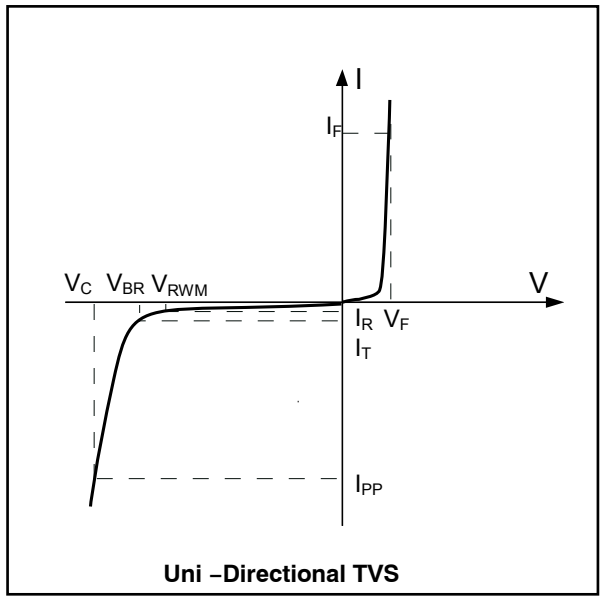
- ► Cellular Handsets & Accessories
- ► Personal Digital Assistants (PDAs)
- ► Notebooks & Handhelds
- ► Portable Instrumentation
- ► Digital Cameras
- ► MP3 Player

MAXIMUM RATINGS(Ta = 25℃)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20s)	Ppp	30	W
Maximum lead temperature for soldering during 10s	TL	260	°C
Storage Temperature Range	Tstg	-40 to +125	°C
Operating Temperature Range	Top	-40 to +125	°C

ELECTRICAL CHARACTERISTICS
(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Uni –Directional TVS

Electrical characteristics (TA=25 °C ,unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	V_{RWM} = 5V			1.0	uA
Reveres breakdown voltage	V_{BR}	I_T=1mA	6.0	7.5		V
Clamping voltage	V_C	Ipp=2A tp=8/20us		11.0		V
Junction capacitance	C_J	V_R = 0V, f = 1MHz (I/O-I/O)		6.5	10.0	pF
		V_R = 0V, f = 1MHz (I/O-GND)			20.0	pF

Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

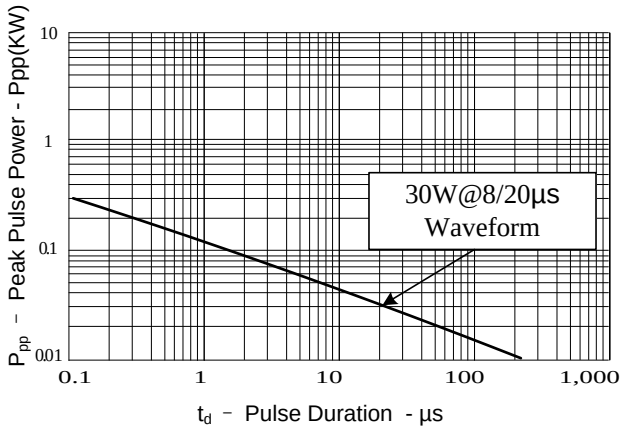


Figure 2: Power Derating Curve

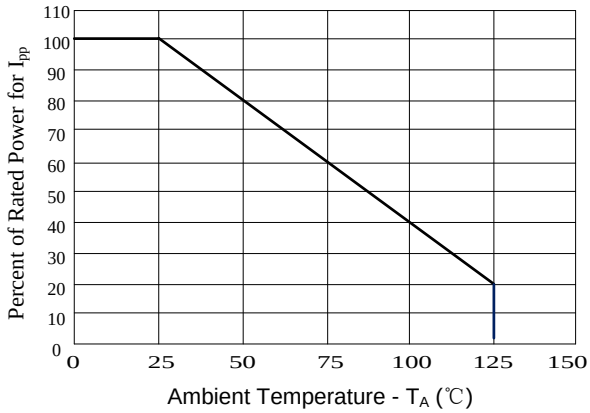


Figure 3: Insertion Loss

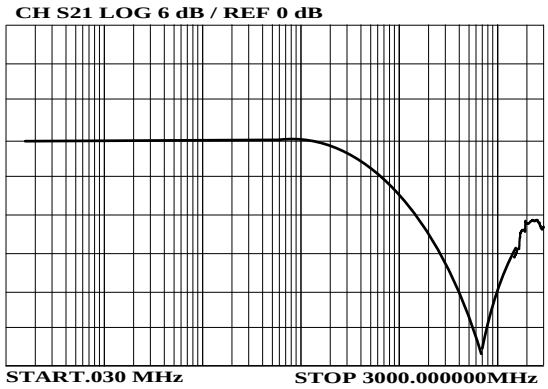
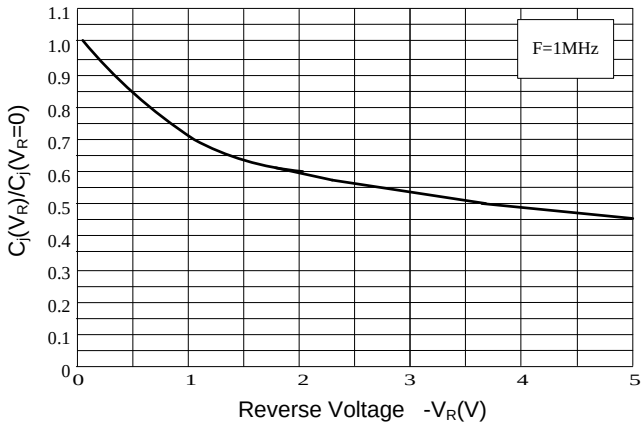


Figure 4: Normalized Junction Capacitance vs. Reverse Voltage



Application Information

The are TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides unidirectional protection; the device is connected as follows:

UNIDIRECTIONAL COMMON-MODE CONFIGURATION

The provides up to four (4) lines of protection in a common-mode configuration as depicted in Figure 1. Circuit connectivity is as follows:

- I/O 1 is connected to Pin 5.
- I/O 2 is connected to Pin 4.
- I/O 3 is connected to Pin 3.
- I/O 4 is connected to Pin 1.
- Pin 2 is connected to ground.

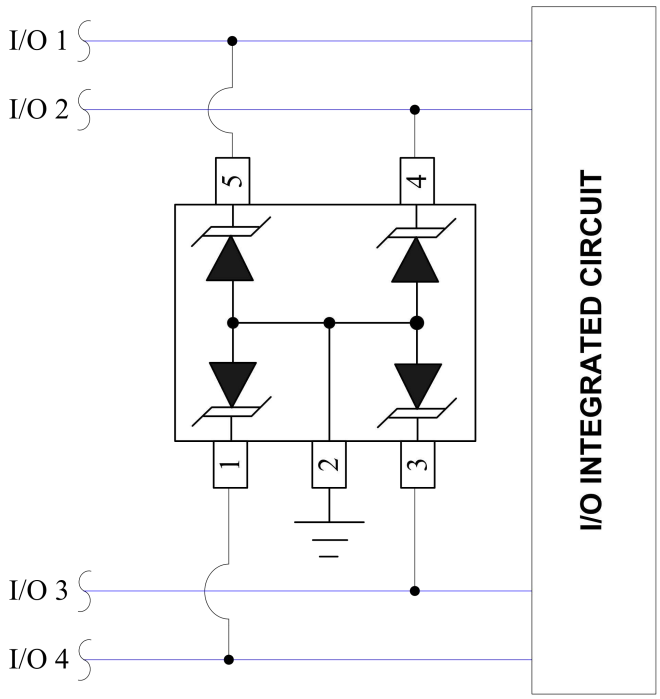


Figure 1 Unidirectional Configuration Common-Mode I/O Port Protections

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection.

The following guidelines are recommended:

＞The protection device should be placed near the input terminals or connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

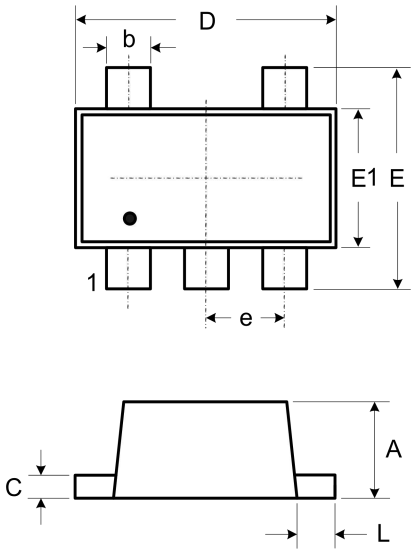
＞ The path length between the TVS device and the protected line should be minimized.

＞ All conductive loops including power and ground loops should be minimized.

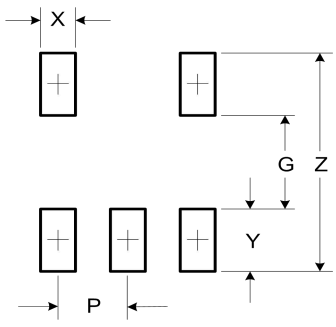
＞ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

＞ Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

Outline Drawing – SOT-553



DIMENSIONS				
SYMBOL	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	0.021	0.024	0.525	0.600
b	0.007	0.011	0.170	0.270
C	0.004	0.006	0.090	0.160
D	0.059	0.067	1.500	1.700
E	0.059	0.067	1.500	1.700
E1	0.043	0.051	1.100	1.300
e	0.018	0.022	0.450	0.550
L	0.004	0.012	0.100	0.300



DIMENSIONS		
DIM	INCHES	MILLIMETERS
Z	0.0708	1.80
G	0.0354	0.90
P	0.0197 TYP	0.50 TYP
X	0.0118	0.3
Y	0.0177	0.45

Notes

1. Dimensioning and tolerances per ANSI Y14.5M, 1985.
2. Controlling Dimension: Inches
3. Dimensions are exclusive of mold flash and metal burrs.