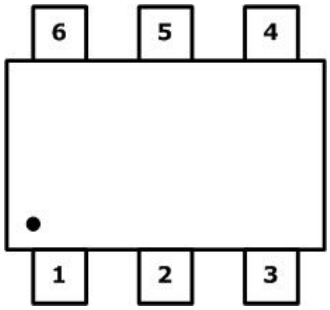
5-Lines Unidirectional Ultra-low Capacitance Transient Voltage Suppressors

Descriptions

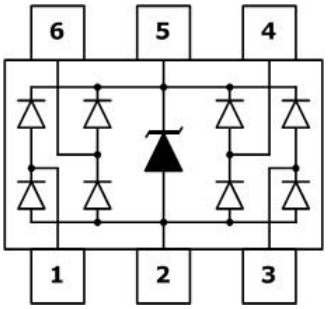
The ESD5M030TR is an ultra-low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, (±30kV air, ±30kV contact discharge).

SOT-26



PIN CONFIGURATION



Features

- Transient protection for high-speed data lines to
  IEC 61000-4-2 (ESD) ±30kV (air), ±30kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- Array of surge rated diodes with internal TVS Diode
- Small package (2.4 x 2.2mm) saves board space
- Protects up to four I/O lines & power line
- Low capacitance **(<1pF)** for high-speed interfaces
- No insertion loss to **2.0GHz**
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology

Applications

- USB 2.0
- USB OTG
- Monitors and Flat Panel Displays
- Gigabit Ethernet
- SIM Ports
- IEEE 1394 Firewire Ports

Order information

Device	Package	Shipping	Marking
ESD5M030TR	SOT-26	3000/Tape&Reel	V05

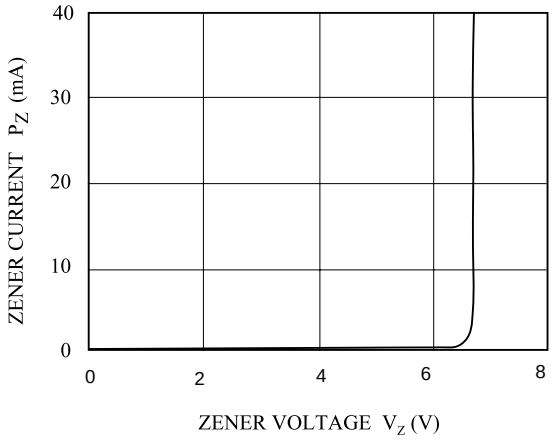
Absolute maximum ratings

Rating	symbol	value	Units
Peak Pulse Current(tp=8/20us)	$I_{pp\ Pin1/3/4/6\sim Pin2}$	4	A
Peak Pulse Current(tp=8/20us)	$I_{pp\ Pin5\sim Pin2}$	20	A
ESD per IEC61000-4-2(Contact)	V_{ESD}	±30	KV
ESD per IEC61000-4-2(Air)		±30	
Operating Temperature	T_J	-55~125	℃
Lead temperature	T_L	260	℃
Storage Temperature	T_{STG}	-55~155	℃

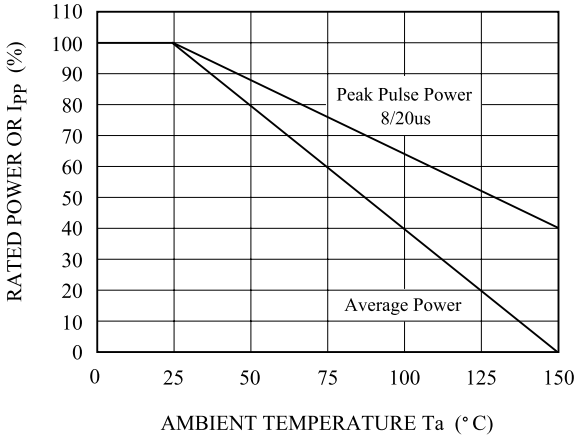
Electrical characteristics (TA=25 oC, unless otherwise noted)

Parameter	Symbol	Conditions	Min.	TYP.	Max.	Units
Reverse stand-off voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	V_{RWM}=5V			1.0	uA
Reveres breakdown voltage	V_{BR}	I_T=1mA	6.0	7.5		V
Clamping voltage	$V_{C\ Pin1/3/4/6\sim Pin2}$	I_{PP}=1A(8/20us)		9.0		V
		I_{pp}= 4A(8/20us)		13.5	15.0	V
Clamping voltage	$V_{C\ Pin5\sim Pin2}$	I_{PP}=1A(8/20us)		8.5		V
		I_{pp}= 20A(8/20us)		20.0	22.0	V
Junction capacitance	$C_{J\ Pin1/3/4/6\sim Pin2}$	VR=0V f=1MHz		0.5	0.8	pF
Junction capacitance	$C_{J\ Pin5\sim Pin2}$	VR=0V f=1MHz		150		pF

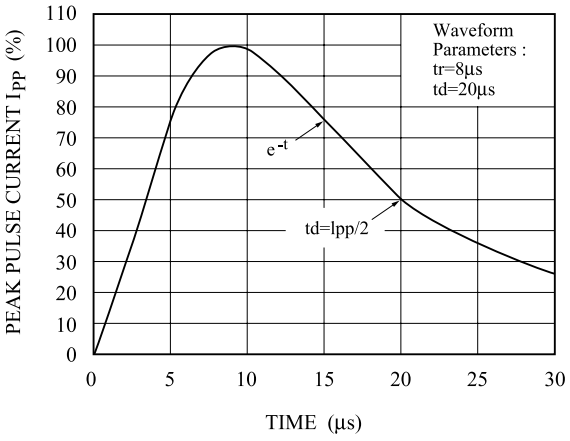
V_Z - I_Z



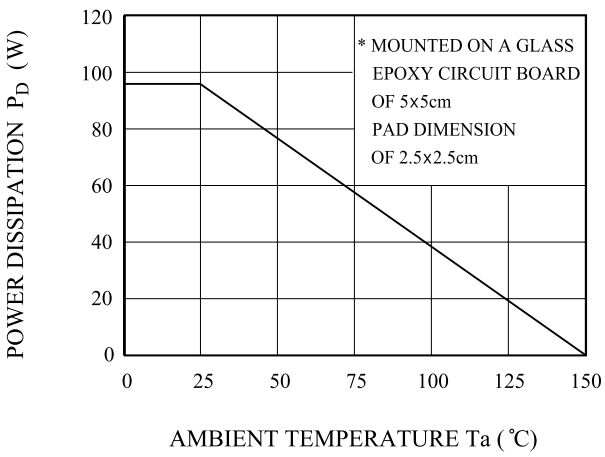
POWER DERATION CURVE



PULSE WAVEFORM



P_D - Ta



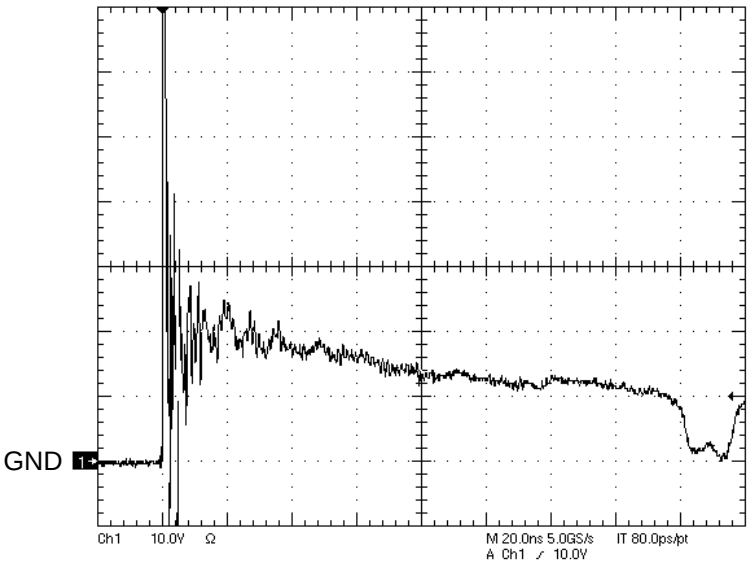


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV Contact per IEC61000−4−2

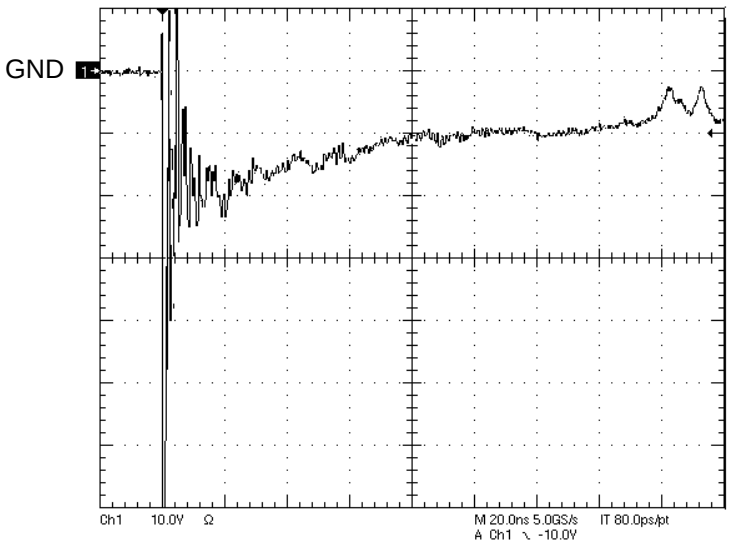


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV Contact per IEC61000−4−2

Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

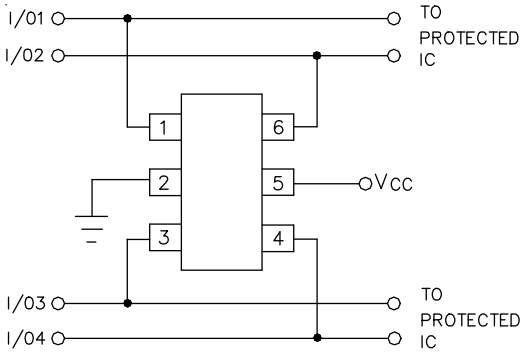
This device is designed to protect data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. Pin 2 should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance.
The positive reference is connected at pin 5. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 5 directly to the positive supply rail (V_{CC}). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, pin 5 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and V_{CC} is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at pins 1, 3, 4, and 6. Pin 2 is connected to ground and pin 5 is not connected.

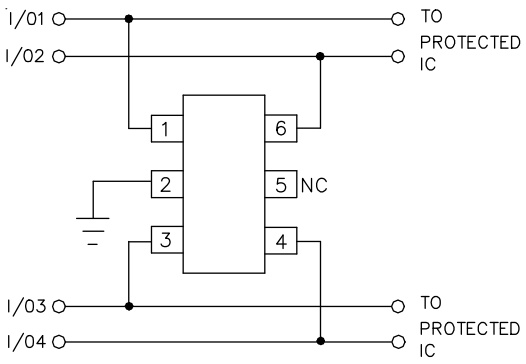
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

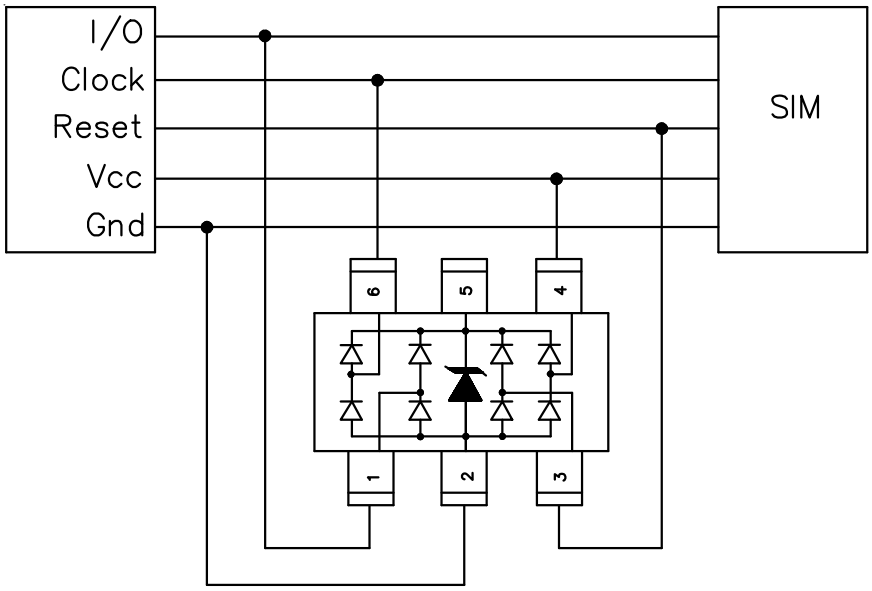
Protection of Four Data Lines and Power Supply Line



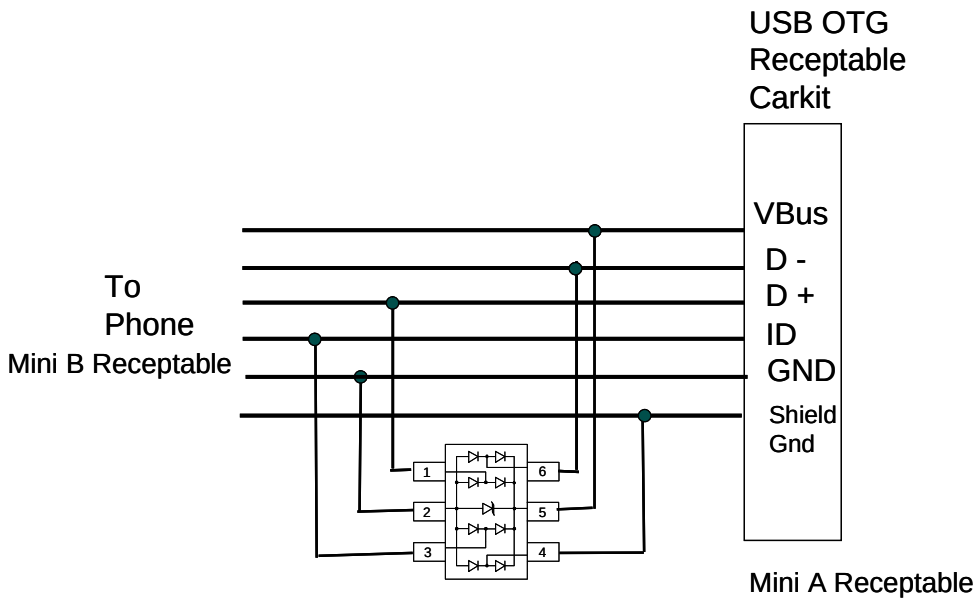
Protection of Four Data Lines Using Internal TVS Diode as Reference



Typical Applications

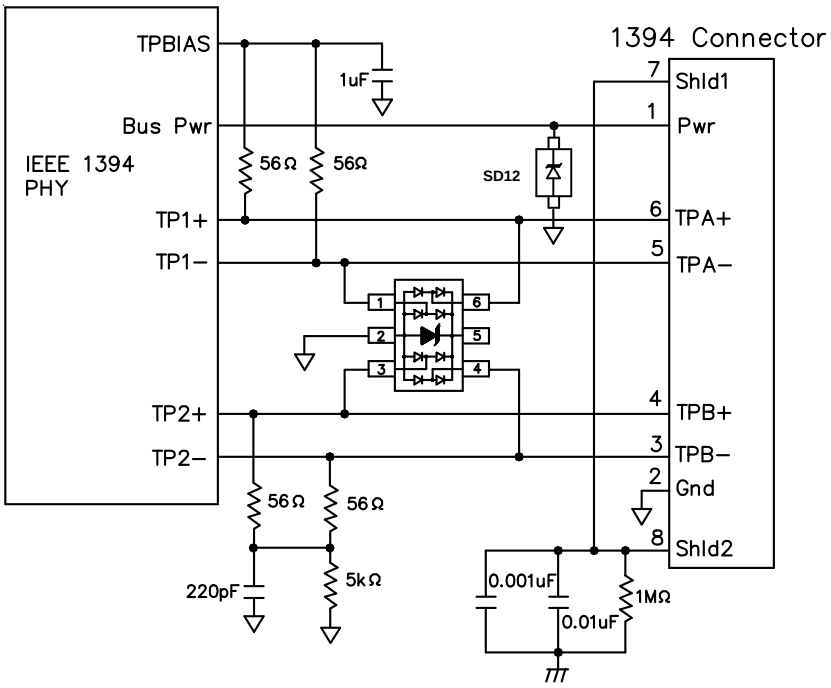


SIM Port - Protection of Three Data Lines and VCC

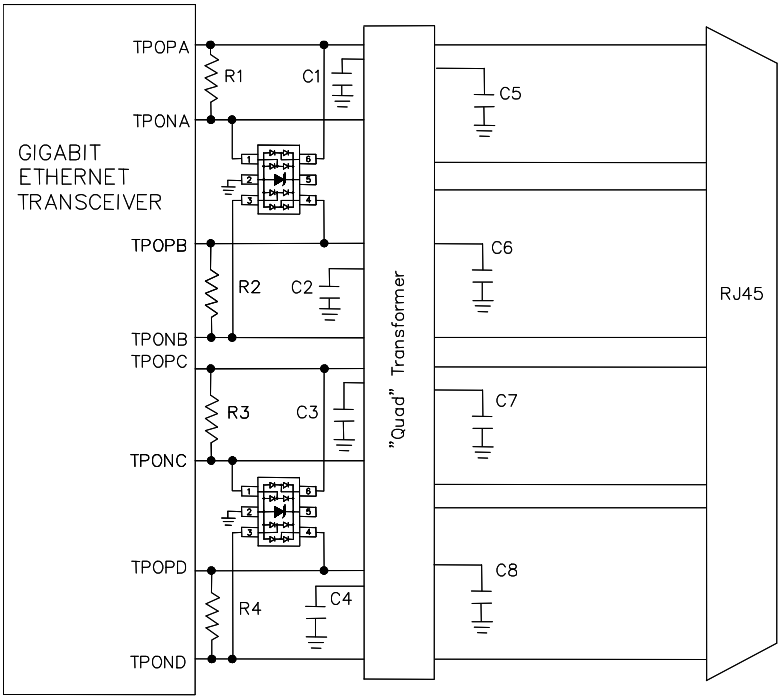


USB OTG Carkit Protection

Typical Applications

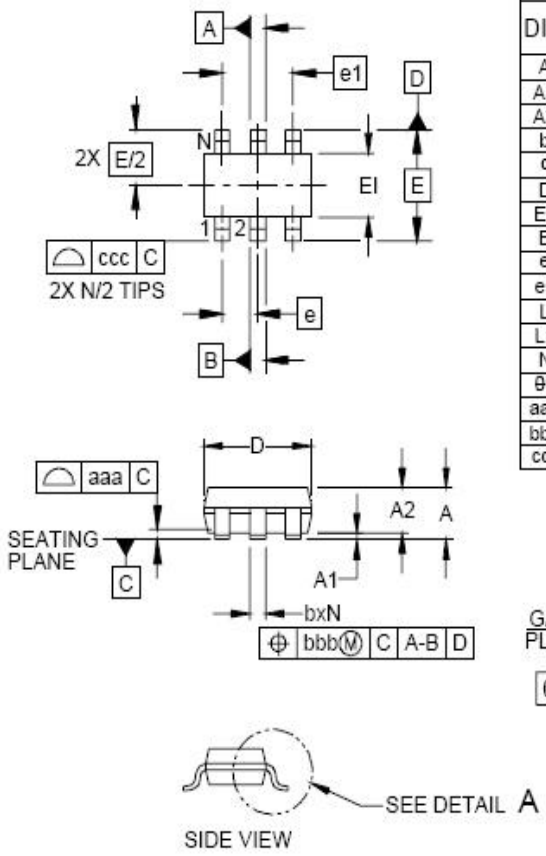


IEEE 1394 Firewire Protection



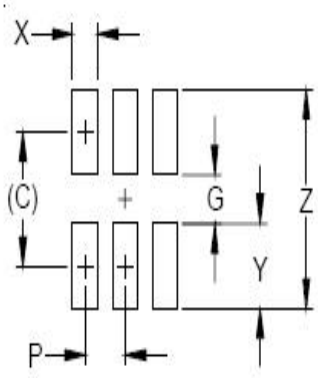
Gigabit Ethernet Protection

SOT-26 PACKAGE OUTLINE & DIMENSIONS



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.035	-	.057	0.90	-	1.45
A1	.000	-	.006	0.00	-	0.15
A2	.035	.045	.051	.90	1.15	1.30
b	.010	-	.020	0.25	-	0.50
c	.003	-	.009	0.08	-	0.22
D	.110	.114	.122	2.80	2.90	3.10
E1	.060	.063	.069	1.50	1.60	1.75
E	.110 BSC			2.80 BSC		
e	.037 BSC			0.95 BSC		
e1	.075 BSC			1.90 BSC		
L	.012	.018	.024	0.30	0.45	0.60
L1	(.024)			(0.60)		
N	6			6		
θ1	0°	-	10°	0°	-	10°
aaa	.004			0.10		
bbb	.008			0.20		
ccc	.008			0.20		

* SOLDERING FOOTPRINT



DIM	INCHES	MILLIMETERS
C	(.098)	(2.50)
G	.055	1.40
P	.037	0.95
X	.024	0.60
Y	.043	1.10
Z	.141	3.60